

Design and Implementation of Doherty Power Amplifier of Global System Mobile (GSM) of Base station

Dr. Saad A. AL Kazzaz

Dept.of Mechatronics Engineering

College of Engineering / Mosul University, Iraq

Kahlan. H. Hamid

Dept.of Electrical Engineering

Abstract

Power amplifier is the main component of wireless communication system. This paper presents the efficiency improvement of linear Power amplifier for GSM base station using Doherty Power Amplifier (DPA). A DPA operating at 900 MHz and a supply voltage of (2.5-3)V. The DPA is a combination of a carrier amplifier biased to class AB mode and a peaking amplifier biased to class C mode. Each amplifier was design by GaAs FET using advance design system software package (ADS). The simulation results of DPA are compared with class AB power amplifier that a show improvement in power added efficiency at output power with acceptable power gain.

Keywords: Doherty Power Amplifier, GaAs FET, Efficiency, GSM, ADS software.

تصميم وتمثيل مكبر قدرة نوع DOHERTY لتطبيقات المحطات الرئيسية لأنظمة الاتصالات المحمولة

كهلان حسان حامد

قسم الهندسة الكهربائية

كلية الهندسة / جامعة الموصل/العراق

د. سعد احمد القزاز

قسم هندسة الميكاترونك

المخلص

يعد مكبر القدرة من الأجزاء المهمة في أنظمة الاتصالات اللاسلكية. في هذا العمل تم تحسين الكفاءة لمكبر القدرة الخطي في المحطات الرئيسية لأنظمة الاتصالات المتنقلة (GSM) باستخدام مكبر القدرة نوع Doherty. يعمل مكبر القدرة Doherty بتردد مقداره (900MHz) والفولتية المجهزة تتراوح ما بين (3-3.6V). يتألف مكبر القدرة نوع Doherty من مكبرين، الأول يطلق عليه المكبر الأساس والثاني المكبر المساعد ويربط المكبرين بمحول ربع طول الموجة وغالبا ما يكون المكبر الأساس صنف AB في حين يكون المكبر المساعد صنف C. حيث تم بناء كل من المكبر الأساس والمساعد بواسطة ترانزستور GaAs FET باستخدام برنامج نظام التصميم المتقدم (ADS). أظهرت نتائج المحاكاة كفاءة قدرة إضافية عالية عند قدرة الإخراج مع كسب مناسب بالنسبة لمكبر القدرة Doherty مقارنة مع مكبر القدرة صنف AB.

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1- Introduction:

The Doherty amplifier is one of the efficiency enhancement techniques for large back-off region from saturation power [1]. The advantages of the Doherty power amplifier are High efficiency and Implementation of linearization [2].

The main purpose of using DPA is to maintain high efficiency over a wide range of input voltage. This system has the potential to deliver high efficiency in base station transmitters [3]. The DPA uses more than one amplifier for different power levels operation as shown in Fig 1.

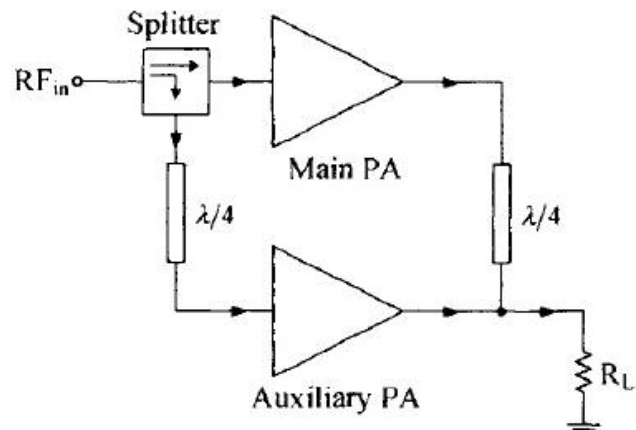


Fig 1. Doherty amplifier architecture

Each amplifier is biased at a different bias condition, and designed to have different load terminations, so that the system as a whole can be optimized for multiple power levels. The conventional Doherty amplifier design uses two amplifiers to compromise between efficiency and linearity in the low-power and high power operation regions. Operation of the DPA does not require manual switching between its component amplifiers. Its operation is controlled by the input power level, without any use of external control or adjustment. This makes it attractive to circuit designers [4].

2- Configuration of Doherty Amplifier:

The DPA consists of carrier and peaking amplifiers connected by a quarter-wave transmission line. The carrier amplifier is typically biased at class A or class AB, and the peaking amplifier is typically biased at class C. The peaking amplifier turns on at power on just before the carrier amplifier starts to go into compression. The current contribution from the peaking amplifier is reducing the effective of load impedance of the carrier amplifier and drawing more current from the device [5].

The operating principle of the Doherty amplifier can be best explained in three stages namely, low, medium and high power levels. Fig 2. represents the block diagram of DPA[6]-[7].

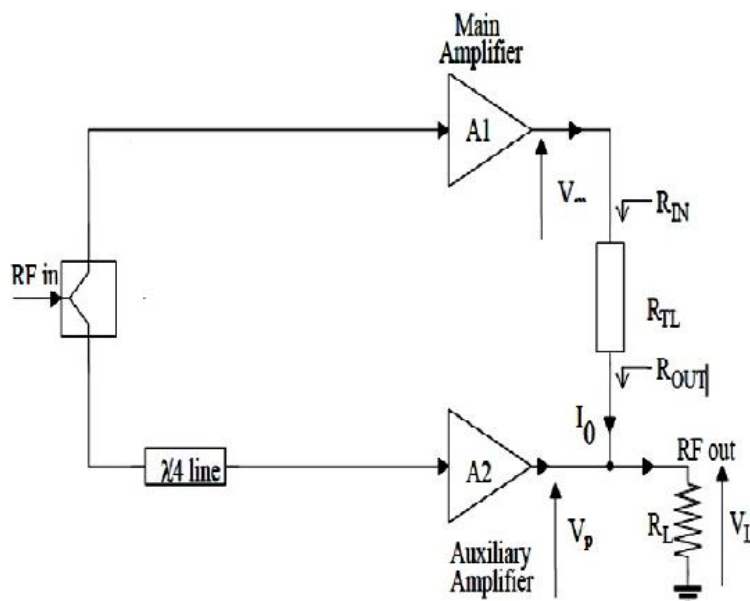


Fig. 2. Block Diagram of Working Principle

Fig.3. shows the ideal characteristics of the voltage and current waveforms of the main and auxiliary amplifier for the entire range of input signal[8].

A. Stage I

During the low cycle of the input signal, the instantaneous amplitude of the input signal is not sufficient to turn on the peak (auxiliary) amplifier and appears as an open circuit is shown in Fig.4. The total low level signal is shown in Fig.4. The total low level signal is received by the carrier (main), which acts as a controlled current source. The carrier (main) amplifier sees the load through the quarter-wave length transmission line and operates exactly the same as an ordinary power amplifier. As the peak (auxiliary) amplifier appeared to be an open circuit, these enable the carrier (main) amplifier to see high output impedance which leads to its saturation while the current has reached only half of its maximum value; and the voltage already reached its maximum value.

Since the voltage has reached its maximum value, the system works with maximum efficiency though it does not deliver the maximum power. The quarter wavelength line enable the carrier (main) amplifier to see high output impedance which leads to its saturation and keeps it maximum voltage at constant condition. The input, output and characteristic impedance of a quarter wavelength transmission line are related by:

$$Z_1 = \frac{Z_T^2}{R_L} \quad (1)$$

B. Stage II

In the region of medium level power, suitable biasing will enable the peak (auxiliary) amplifier to turn on when the carrier (main) amplifier is saturated as shown in Fig. 5. At this point the peak (auxiliary) amplifier will act as a controlled current source while the carrier (main) amplifier acts as a controlled voltage source. Once the peak (auxiliary) amplifier starts to supply current, the current will increase the impedance at Z_0 seen by the quarter wavelength (According to the active load pull technique). However, increasing in the impedance of Z_0 results in decreasing the impedance of Z_1 , which is the impedance seen by the carrier (main) amplifier.

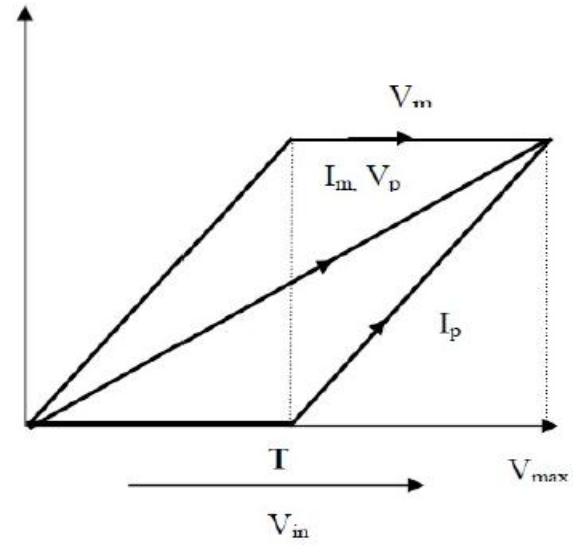


Fig. 3. Current and Voltage Characteristics of Doherty Power Amplifier

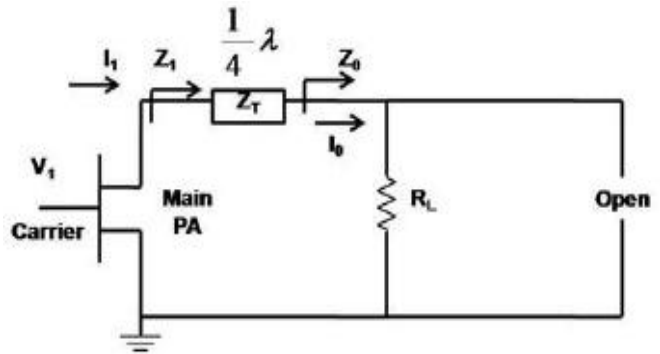


Fig. 4. Low level input signal

This causes the main amplifier output voltage to remain constant without reaching saturation whilst increasing the output current from the main amplifier, this means, the increase in the output current increases the resultant output power.

The importance of quarter wavelengths at this stage causes the impedance seen by the carrier (main) amplifier to decrease as the peak (auxiliary) amplifier turns on, this guarantees highly efficient power combining.

$$Z_1 = \frac{Z_T^2}{R_L \left(1 + \frac{I_2}{I_0}\right)} \quad (2)$$

And Z_2 is

$$Z_2 = R_L \left(1 + \frac{I_0}{I_2}\right) \quad (3)$$

C. Stage III

Finally, when both amplifiers carrier and peak contribute to the same amount of power to load, the Doherty amplifier is working at the high power level, i.e. $I_0 = I_2$ as shown in Fig.5. In this region when $I_0 = I_2$. and by substituting $I_0 = I_2$ in Z_1 and Z_2 equation at the high level input power is [9]:

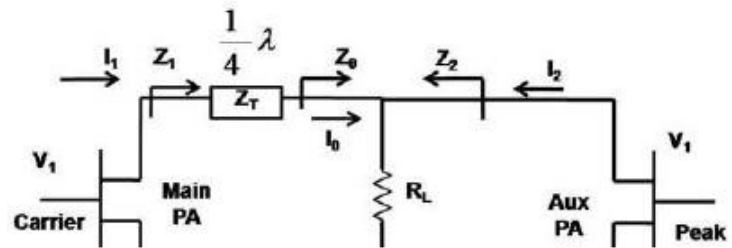


Fig. 5. Medium and high level input signal

$$Z_1 = \frac{Z_T^2}{2R_L} \quad (4)$$

$$Z_2 = 2R_L \quad (5)$$

3- Design Approach:

Here, we have a DPA implemented using a class AB structure, with the class C joined by a lumped element equivalent taken from a quarter-wave transmission line. A two stage DPA is analyzed and its performance is compared with the conventional class AB power amplifier. The design implementation of class AB P.A with a 900 MHz input RF frequency is shown in Fig.6. The D.C. voltage is equal to 3 V and the biasing voltage is equal to -2V.

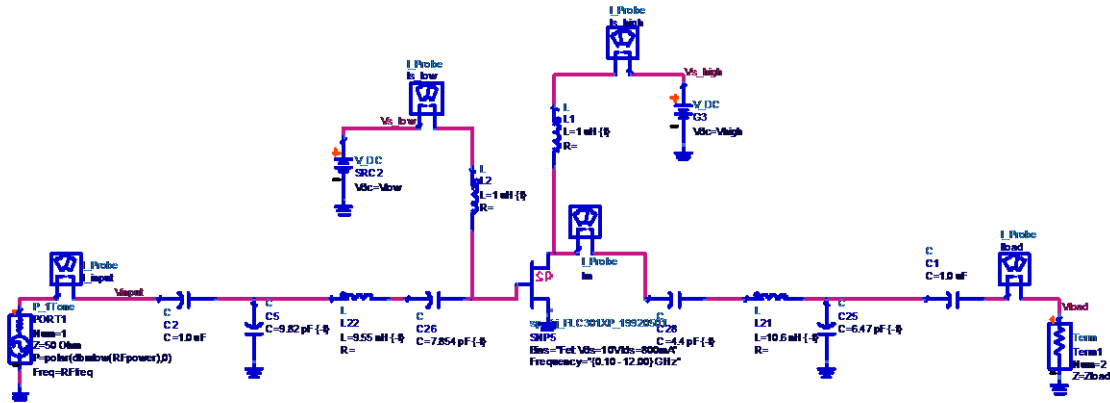


Fig.6. Implementation of Class AB PA

A similar approach was applied for the class C amplifier. As shown in Fig.7 the schematic of Doherty Amplifier, the class C amplifier is placed at the bottom and the class AB amplifier is located on the top. The D.C. voltage is equal to 3 V and the biasing voltage is shown in table.1.

Table.1. biasing voltage

Class of Operation	Main stage Class AB	Auxiliary Stage Class C
Gate Voltage	-2	-3

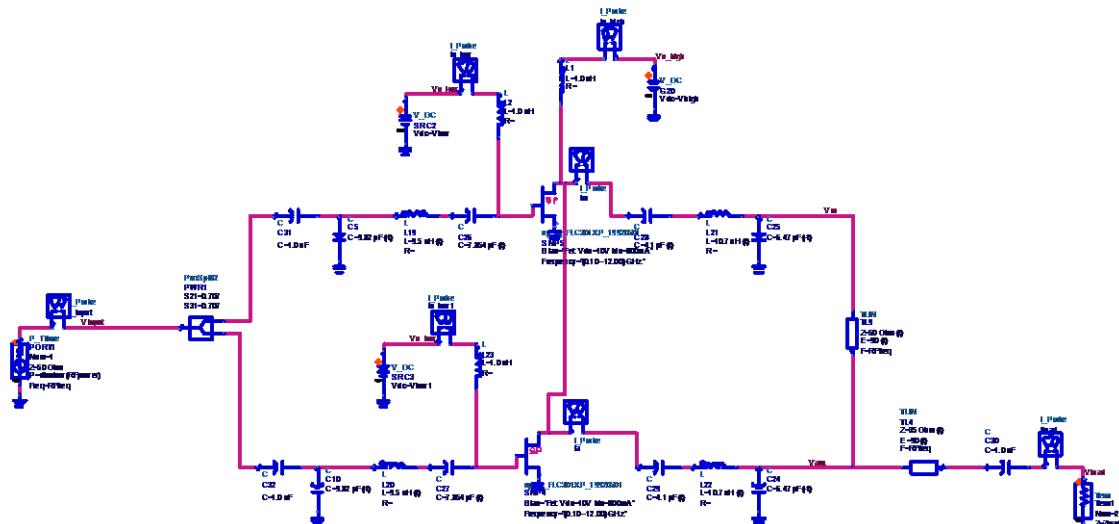


Fig.7. Implementation of Doherty PA

4- Simulation Results

This section provides a design procedure of the two stage Doherty topology. Such as DC simulation, bias point selection, S-parameter simulation, matching circuit design, load pull characterization.

A. DC Simulation

The first step of simulation is simply to determine the DC bias condition of the transistor. The datasheet specifies that the gate-source threshold voltage is from 0V to -3.0V and the drain-source voltage is recommended to operate at 3V. Thus, the simulation is set up to vary the drain-source voltage from 0V to 5V and the gate-source voltage is varied by the given range. The simulation generated an I-V curve for the transistor displaying the load line as shown in Fig.8.

The I-V curve of the transistor will be used to determine the DC bias condition of the amplifier. For the amplifier design simulation, the supply drain-source voltage equal to 3V and with gate-source voltage is chosen to be -2V. This bias condition, as the I-V curve indicates, is meant that the amplifier is class AB type. Fig.9 represents the range of gate voltages and the corresponding mode of operation with a drain voltage of 3V.

B. Load and Source Pull Simulation

The next step in designing the amplifier is to characterize the input and the output impedance of the transistor. This is because to obtain the best power added efficiency, the transistor needs to be very well matched at given frequency and driving input power.

ADS providing the load-pull and source pull simulation tool to find the suitable load impedance and source impedance for the transistor to achieve maximum efficiency. The result obtained from these simulations shows that the transistor needs to see an impedance of $11.528 + j13.2$ ohms at the output and $9.126 + j11.881$ ohms at the input. This result is shown in Fig.10 and Fig.11.

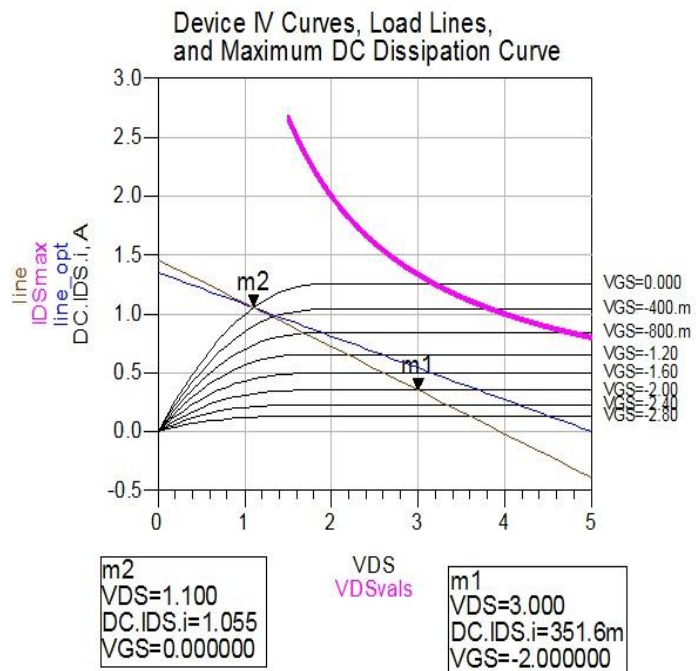


Fig.8.shows the output characteristics of the GaAS FET

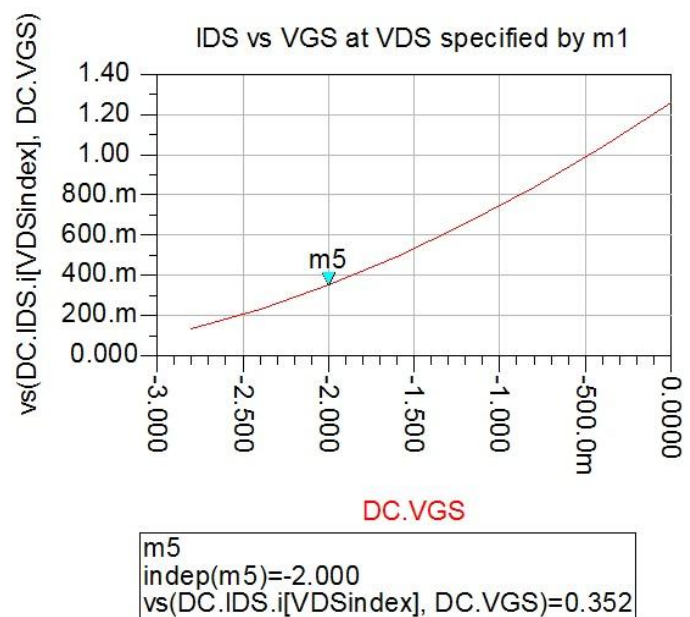


Fig.9. shown the transfer characteristics of GaAs

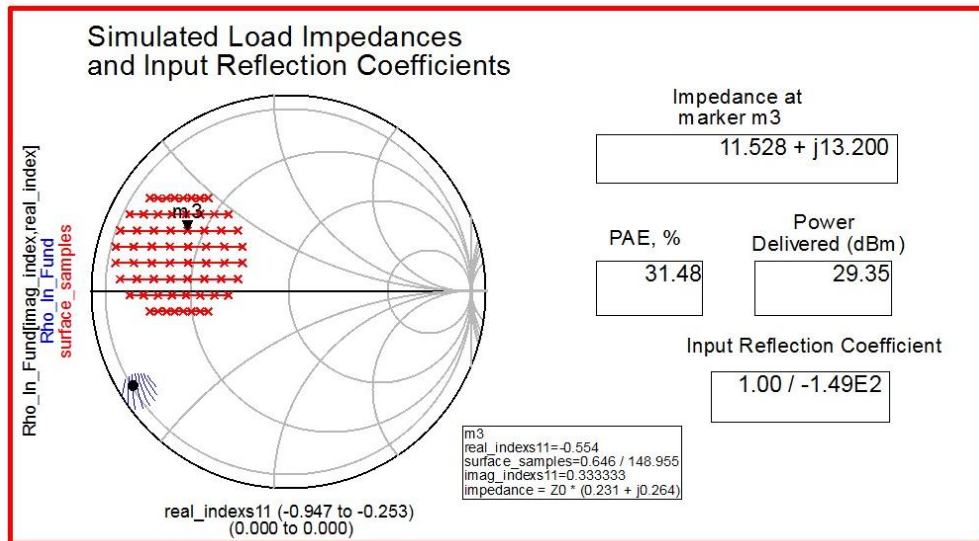


Fig.10. the output power and efficiency at different load impedance

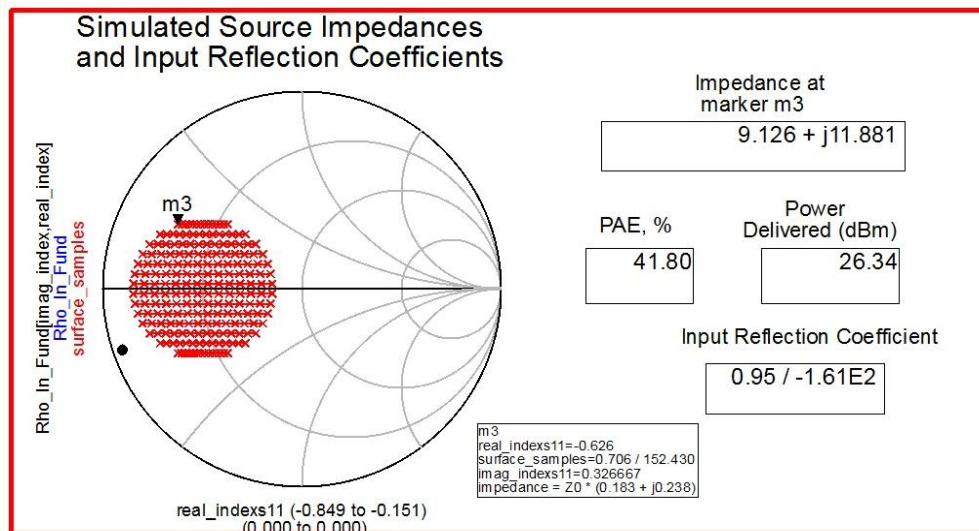
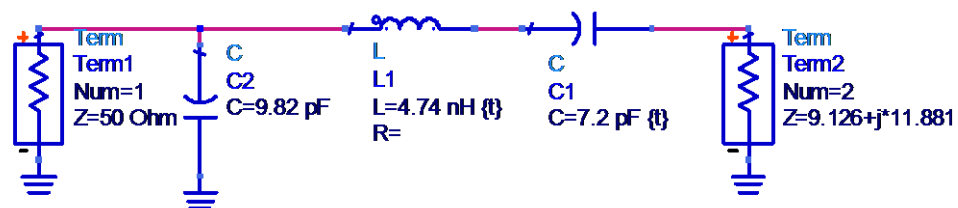


Fig.11. the output power and efficiency at different source impedance

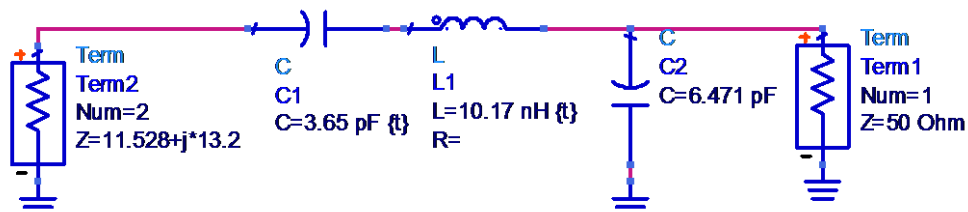
C. Input and Output Matching Network

The matching network design is aimed to work over a large bandwidth as possible [10]. Input and output matching can be provided using a simple discrete element matching network such as L-match, T-match or π -match. In this design, the Q-factor of the inductor used to calculate the matching network is equal to 5.

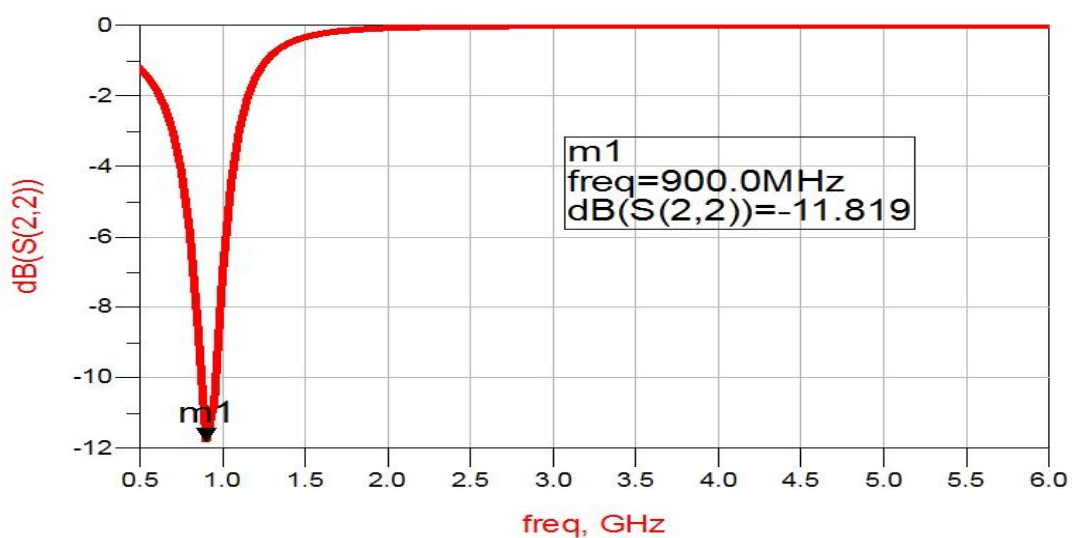
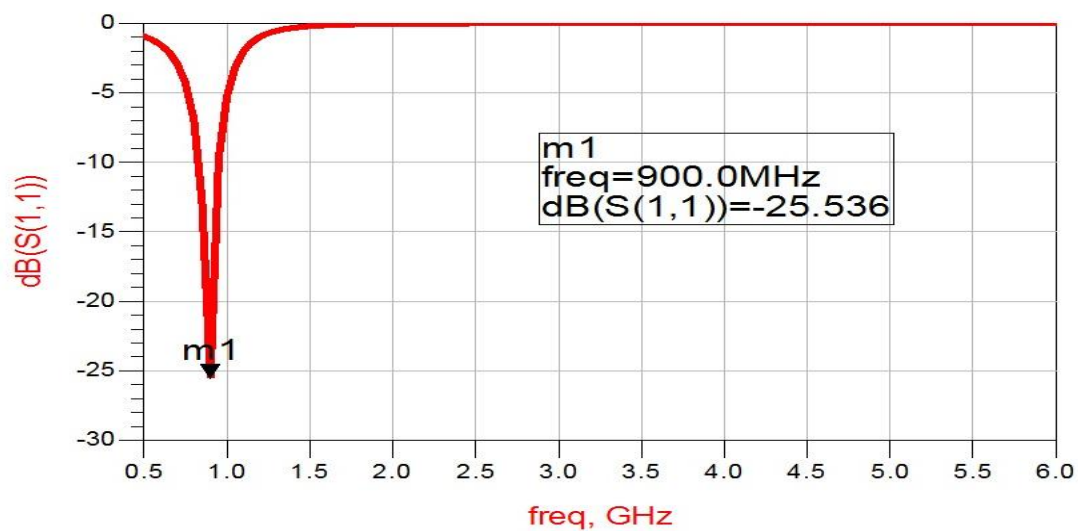
The ADS Design Guide tool “Lumped Multi-Element Z-Y Matching Networks” was used to determine lumped element output and input matching networks that transformed 50 ohms into the desired optimum load and source impedance values. Fig.12 through Fig.14 show the matching networks (MNs) and results.



Fig(12) Input Matching



Fig(13) Output Matching



Fig(14) input and output matching results

D. S-Parameter Simulations:

• S-parameter Simulation of a Class AB PA

In S-parameter simulation of class AB, S11 the reflection coefficient, S21 the power gain, were shown in Fig.15. From the figure, its center frequency is at 900Mhz. the S(1,1)-insertion loss is below -7.727dB and the S(2,1) the power gain is about 19.728dB. The bandwidth is about 100 MHz From the data; the input impedance is matched to 50 Ohm.

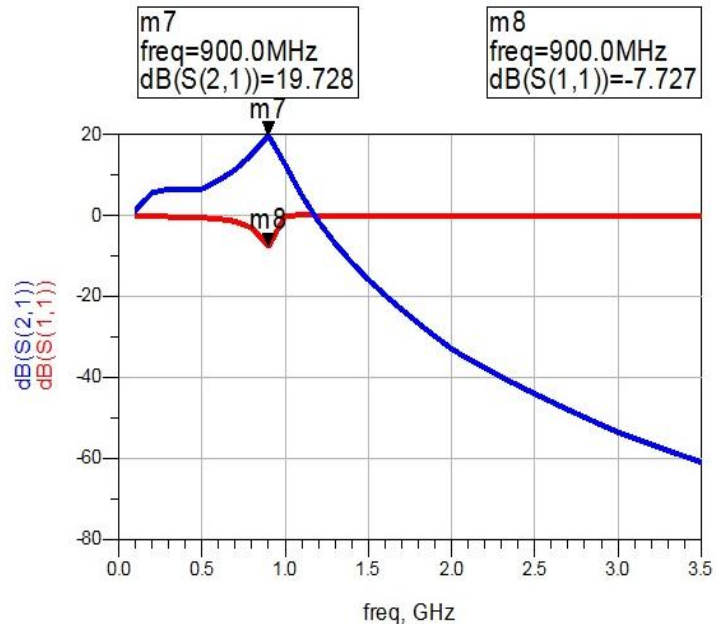


Fig.15. Simulation result of the S-parameter of Class AB PA

In S-parameter simulation of Doherty PA, S(1,1)-the reflection coefficient, S(2,1)-the power gain, were shown in Fig.16. From the figure, its center frequency is at 900Mhz. the S(1,1)-insertion loss is below -7.667dB and the S(2,1) the power gain is about 18.619dB. The bandwidth is about 100 MHz.

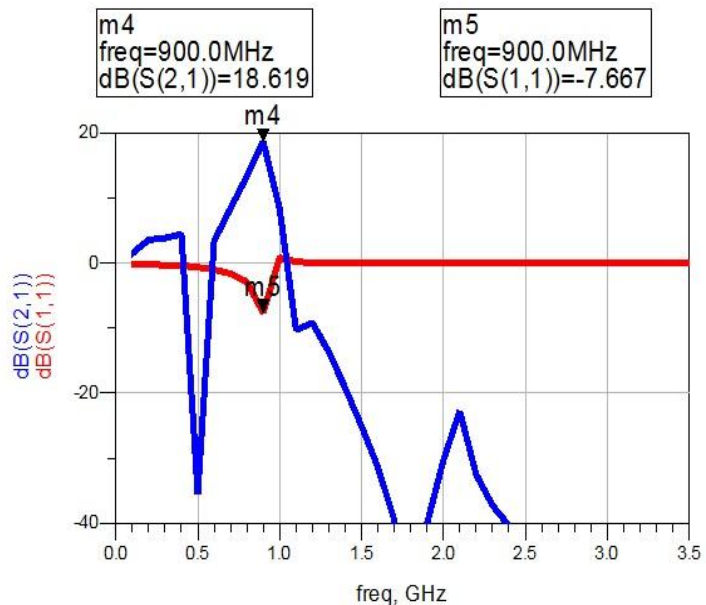


Fig.16. Simulation result of the S-parameter of Doherty PA

E. Harmonic Terminations

• Harmonic Terminations of a Class AB PA

Fig.17 shows the efficiency versus the output power. From the figure, the PAE increase with the input power and reach the peak efficiency for 51.597%.

Fig.18 shows the efficiency versus the output power. From the figure, the PAE increase with the input power and reach the peak efficiency for 57.022%.

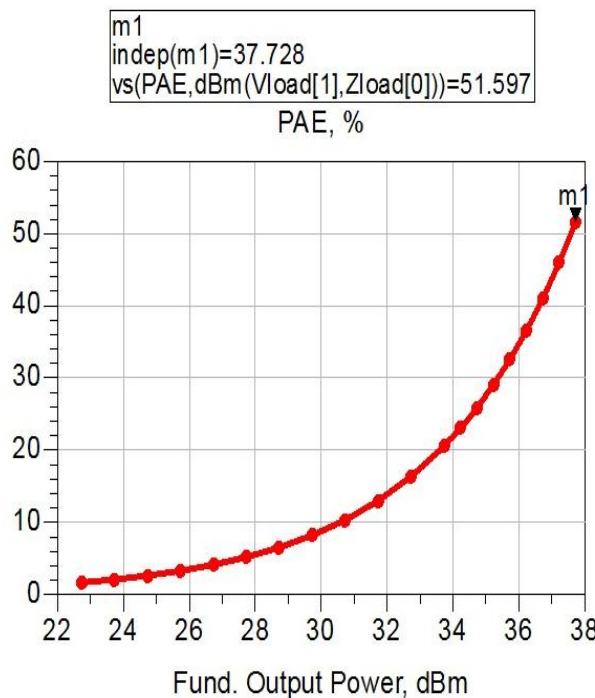


Fig.17. shows the efficiency versus the output power

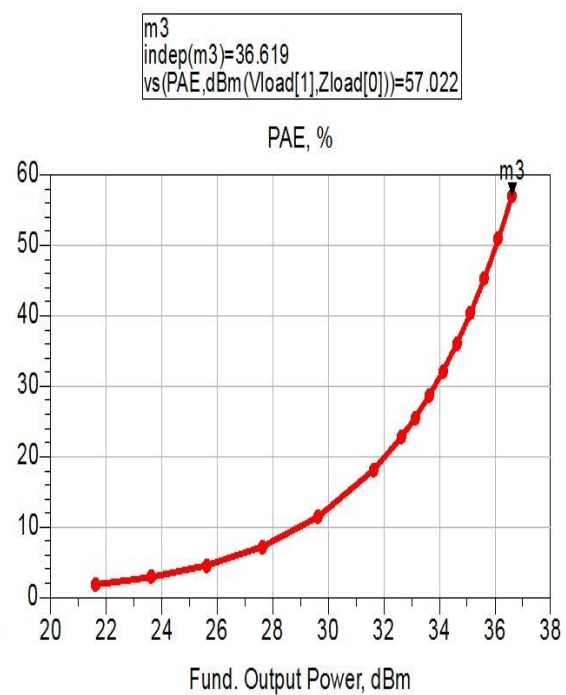


Fig.18. shows the efficiency versus the output power

• Harmonic Terminations of a Doherty PA

The simulation result of DPA compared with class AB power amplifier is shown in Table.2.

Table.2.simulation results

Type of Amplifier	Doherty(AB type)	Class AB P.A
Frequency(MHz)	900 MHz	900 MHz
Band (MHz)	100 MHz	100 MHz
Gain (dB)	7.757 dB	8.57 dB
Out Power(dBm)	36.619 dBm	37.728 dBm
PAE (%)	57.022 %	51.597

5- Conclusions:

It is extremely hard to get both high efficiency and good linearity in the power amplifier. This paper presents efficiency improvement of linear Power amplifier of GSM base station using Doherty Power Amplifier (DPA), consists of class AB power amplifier in parallel with class C power amplifier. The results show that there is an improvement in efficiency of Doherty power amplifier more than (5.425%) as compared to stand alone class AB power amplifier. This technique is suited to enhance the efficiency for the linear power amplifier of the GSM.

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The work was carried out at the college of Engineering. University of Mosul